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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,123	04/08/2004	Blake W. Little	65744/P018US/10404217	8209

29053 7590 09/16/2009

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EXAMINER	
TRAN, PHUC H	
ART UNIT	PAPER NUMBER
2416	

MAIL DATE	DELIVERY MODE
09/16/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,123	LITTLE ET AL.	
	Examiner	Art Unit	
	PHUC H. TRAN	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26 and 29-31* is/are rejected.

7)☒ Claim(s) *27,28 and 32-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal brief filed on 4/29/2009, PROSECUTION IS HEREBY REOPENED. A new ground of rejection set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 12-14, and 17are rejected under 35 U.S.C. 101 as not falling within one of the four statutory categories of invention. While the claims recite a series of steps or acts to be performed, a statutory "process" under 35 U.S.C. 101 must (1) be tied to particular machine, or (2) transform underlying subject matter (such as an article or material) to a different state or

thing. See page 10 of In Re Bilski 88 USPQ2d 1385. The instant claims are neither positively tied to a particular machine that accomplishes the claimed method steps nor transform underlying subject matter, and therefore do not qualify as a statutory process. The method including step of configuring an ASIC is broad enough that the claim could be completely performed mentally, verbally or without a machine nor is any transformation apparent. For example the step of "configuring an ASIC adapted for use in a plurality systems" is not tied to particular machine to configure the ASIC.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 2-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding to claims 2-5, the N and M in claims are failing to particularly point out what value of M and N are and the different between N and M (N = M or N>M or N<M). Therefore, the value of N and M should be defined in the claims.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 6, 7, and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Leavitt et al. (U.S. Patent No. 6491634).

- With respect to claim 1, Leavitt teaches a system comprising: an application specific integrated circuit (ASIC) adapted for use in a plurality of systems (e.g. block 210 in fig. 2), wherein the system is one of the plurality of systems, and each system has a circuit configuration that uses a different number of signal channels for further processing by said application specific integrated circuit (e.g. signal channels in Fig. 1-7 that communicates in the system between blocks as in Fig. 2).

- With respect to claim 6, Leavitt teaches wherein said ASIC comprises: a circuit configurable to provide a cross point switch function in a first configuration of said circuit configurations and to provide a signal summer function in a second configuration of said circuit configurations (e.g. Fig. 7A shows the cross point switch function and summer for signal).

- With respect to claim 7, Leavitt discloses wherein said cross-point switch function comprises selectively routing signal channels to one or more beam formers (e.g. signals from ASIC to beam former in Fig. 2).

- With respect to claim 10, Leavitt teaches a system comprising: an application specific integrated circuit (ASIC) adapted for use in a plurality of circuit configurations (e.g. block 210 in Fig. 2), said circuit configurations providing for different numbers of signal channels for further processing using same circuitry of said application specific integrated circuit (e.g. signal channels in Fig. 1-7 that communicates in the system between blocks as in Fig. 2); wherein the ASIC is included in an application comprising a transducer (e.g. block 106 in Fig. 1), a beam

former (e.g. blocks 218 and 226 in Fig. 2), and a data path, and wherein the data path is in communication with the ASIC, the transducer, and the beam former (e.g. links in Fig. 2).

- With respect to claim 11, Leavitt discloses wherein the application further comprises a signal processing unit external to the data path and in communication with the data path at a number of points thereon and is operable to capture and insert information in the data path at each of those number of points (e.g. processor 258 in Fig. 2).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2-3, 5, 8, 9, and 25-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leavitt et al. (U.S. Patent No. 6491634) in view of Henderson et al. (U.S. Patent No. 6695783).

- With respect to claim 2, Leavitt teaches wherein said ASIC (as in Fig. 2) discloses all the aspect of the claimed invention as set forth above but fails to teach a plurality of multiplexors providing N to M signal multiplexing, wherein in a first configuration of said circuit configurations said ASIC is configured to provide N to M signal multiplexing, and wherein in a second configuration of said circuit configuration said ASIC is configured to provide N to M/2 signal multiplexing. Henderson teaches a plurality of multiplexers (as in Fig. 6) for processing

signals. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to implement the multiplexors of Henderson into the ASIC (block 210 of Leavitt) for processing to reduce signals.

- With respect to claims 3, and 26, Leavitt teaches wherein said ASIC (as in Fig. 2) discloses all the aspect of the claimed invention as set forth above but fails to teach the multiplexer that Henderson teaches wherein said plurality of multiplexors include N signal inputs, M signals outputs (e.g. in fig. 6 number of input and number of output), at least one select signal input, and at least one enable signal input, said enable signal input being utilized in providing said N to M/2 signals multiplexing of said second configuration (Fig. 6-8 as signals input and selected, it is also well known in the art that the multiplexer has input, output signals, select signal and enable signal). Therefore, it would have been obvious to combine for the reason as set forth above with respect to claim 2.

- With respect to claim 5, Leavitt teaches wherein said ASIC (as in Fig. 2) discloses all the aspect of the claimed invention as set forth above but fails to teach the multiplexer which Henderson discloses at least one of said select signals input and said enable signal input comprise a digital serial control bus (e.g. buses in fig. 8). Therefore, it would have been obvious to combine for the reason as set forth above with respect to claim 2.

- With respect to claim 8, Leavitt teaches wherein said ASIC (as in Fig. 2) discloses all the aspect of the claimed invention as set forth above but fails to teach the summer function which Henderson also teaches wherein the signal summer function comprises a symmetric signal summing operation (e.g. block 76, 86, 116, and 126 in Fig. 8). Therefore, it would have been obvious to combine for the reason as set forth above with respect to claim 2.

- With respect to claim 9, Leavitt teaches wherein said ASIC (as in Fig. 2) discloses all the aspect of the claimed invention as set forth above but fails to teach the symmetric signal summing which Henderson teaches wherein the symmetric signal summing operation comprises summing one or more signals that are determined to be of similar weight and delay (see col. 3, lines 30-35). Therefore, it would have been obvious to combine for the reason as set forth above with respect to claim 2.

- With respect to claims 25, and 29, Leavitt teaches an apparatus comprising: a sonogram imaging (e.g. the system in fig. 1) system including: a transducer (block 106 in Fig. 1); a beam former (e.g. block 218 and 226 in Fig. 2); a data path including a plurality of information channels connecting the transducer to the beam former (e.g. data path in fig. 2); and an ASIC in communication with the data path between the transducer and the beam former (e.g. block 210 in fig. 2). Leavitt fails to teach ASIC including circuitry operable as a bank of multiplexors to decrease a number of the information channels from the transducer to the beam former. Henderson teaches a plurality of multiplexers (as in Fig. 6) for processing signals. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to implement the multiplexors of Henderson into the ASIC (block 210 of Leavitt) for processing signals.

- With respect to claim 30, Leavitt teaches wherein said ASIC (as in Fig. 2) discloses all the aspect of the claimed invention as set forth above but fails to teach the circuitry included by the ASIC comprises a summation bus and cross-point switch circuitry. Henderson teaches the summation bus (Fig. 8 shows summation of bus and the switch circuitry of signals from FIFO). Therefore, it would have been obvious to a person of ordinary skill in the art at time of the

invention was made to implement the Henderson's ASIC into Leavitt's ASIC for multiplexing and switching signals in the system.

- With respect to claim 31, Leavitt teaches wherein said ASIC (as in Fig. 2) discloses all the aspect of the claimed invention as set forth above but fails to teach wherein the summation bus is operable to decrease a number of information channels between the transducer and the beam former. Henderson teaches the multiplexers (in Fig. 8 shows the multiplexer from 2:1), Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to implement the ASIC of Henderson to the ASIC of Leavitt for multiplexing signals in the system.

9. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leavitt et al. (U.S. Patent No. 6491634) in view of Sipin (U.S. Patent No. 5000052).

- With respect to claims 12 and 13, Leavitt teaches a method configuring an ASIC adapted for use in a plurality of systems (e.g. block 210 in fig. 2), wherein each system has a circuit configuration that uses a different number of channels, to provide said determined number of channels (e.g. signal channels in Fig. 1-7 that communicates in the system between blocks as in Fig. 2). Leavitt fails to teach determining a number of channels for use in a data path. Sipin teaches the number channels in the path (see col. 14, lines 45-46) for determining the capacity of the flow path. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to implement the method of determining number of channels in the path for determining the capacity of the path.

10. Claims 14, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leavitt et al. (U.S. Patent No. 6491634) and Sipin (U.S. Patent No. 5000052) in further view of Henderson et al. (U.S. Patent No. 6695783).

- With respect to claim 14, Leavitt and Sipin teach wherein said ASIC (as in Fig. 2) discloses all the aspect of the claimed invention as set forth above but fails summing data on each of at least two channels by the ASIC. Henderson teaches the summation bus (Fig. 8 shows summation of bus signals from FIFO). Therefore, it would have been obvious to a person of ordinary skill in the art at time of the invention was made to implement the Henderson's ASIC into Leavitt's ASIC for multiplexing and switching signals in the system.

- With respect to claim 19, Leavitt and Sipin teach wherein said ASIC (as in Fig. 2) discloses all the aspect of the claimed invention as set forth above but fails to teach the multiplexors decrease a number of information channels between the transducer and the beam former. Henderson teaches the multiplexers (in Fig. 8 shows the multiplexer from 2:1), Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to implement the ASIC of Henderson to the ASIC of Leavitt for multiplexing signals in the system.

- With respect to claim 20, Leavitt and Sipin teach wherein said ASIC (as in Fig. 2) discloses all the aspect of the claimed invention as set forth above but fails to teach wherein the multiplexors are 2:1 multiplexors, and wherein operating as a plurality of multiplexors comprises selectively enabling one of every two 2:1 multiplexors, thereby providing 4:1 multiplexing functionality. Henderson teaches wherein said plurality of multiplexors include 2:1 multiplexors (e.g. in fig. 6 number of input and number of output), at least one select signal input, and at least

one enable signal input, said enable signal input being utilized in providing said N to M/2 signals multiplexing of said second configuration (Fig. 6-8 as signals input and selected, it is also well known in the art that the multiplexer has input, output signals, select signal and enable signal). Therefore, it would have been obvious to combine for the reason as set forth above with respect to claim 2.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHUC H. TRAN whose telephone number is (571)272-3172. The examiner can normally be reached on M-F (8-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, CHI PHAM can be reached on (571) 272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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